

What is claimed is:

1. A method of operating a computer system to design an application specific processor (ASP) comprising:

defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor;

generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure;

entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table; and

using the register definition file to create in silicon the registers of the ASP.

2. A method according to claim 1, wherein each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element.

3. A method according to claim 1, wherein each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element.

4. A method according to claim 1, wherein the register definition table includes the word location of the register within a memory map for access during simulation of the ASP.

5. A computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP), wherein the computer system comprises an input means for receiving a

plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure;

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefine sectors of a register definition table; and

wherein the computer system further comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP.

6. A computer system according to claim 5, wherein the input means comprises means for receiving a physical recording device holding the input file for each peripheral.

7. A computer system according to claim 5, wherein the output means comprises means for loading the register definition file onto a physical recording device.

8. A computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language, and to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers.

9. A register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word

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9 location of the register within a memory map for access during simulation of an ASP implementing the registers.

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